Amendments to the Claims:

This Listing of Claims will replace all prior versions and listings of claims in this Application.

1. (Currently Amended) A method of forming a MIM capacitor, comprising the steps of:

~~providing a structure having a metal structure formed thereover;~~

~~forming a dielectric layer over the metal structure;~~

~~forming a top layer over the dielectric layer;~~

forming a capacitance trench ~~through the top layer and into the~~ within a dielectric layer formed over a substrate; the capacitance trench having opposing side walls and a bottom;

forming respective bottom electrodes [[over]] along the ~~capacitance trench~~ opposing side walls;

forming a capacitance dielectric layer along [[over]] the respective bottom electrodes~~, the bottom of the capacitance trench and the remaining top layer~~;

forming at least one dual damascene opening that exposes ~~respective opposing initial via openings adjacent the capacitance trench;~~

~~forming respective trench openings above, continuous and contiguous with the lower portions of the respective opposing initial via openings and exposing~~ portions of [[the]] an underlying metal structure ~~to form respective opposing dual damascene openings~~; and

~~forming~~ depositing metal and planarizing to form planarized metal portions within[[:]]

the dual damascene openings; and

the capacitance trench to form a top electrode[[;]]

~~to complete formation~~ of the MIM capacitor.

2. (Currently Amended) The method of claim 1, further comprising forming the dielectric layer over the underlying metal structure and forming a top layer over the dielectric layer prior to said forming a capacitance trench, and wherein

the capacitance trench is formed to extend through the top layer,

the capacitance dielectric layer is further formed along the bottom of the capacitance trench and remaining portions of the top layer, and

forming at least one dual damascene opening comprises forming initial via openings adjacent the capacitance trench then forming respective trench openings above, continuous and contiguous with lower portions of the respective via openings to form respective opposing ones of said at least one dual damascene opening ~~wherein the structure is a silicon substrate, a germanium substrate, a semiconductor wafer or a semiconductor substrate~~.

3. (Currently Amended) The method of claim 2 [[1]], wherein the metal structure is comprised of copper, aluminum or gold; the dielectric layer is comprised of an oxide material having a dielectric constant of less than about 3.0, silicon oxide or FSG; the top layer is comprised of silicon oxynitride; the bottom electrodes are comprised of TaN or Tin; the capacitance dielectric layer is comprised of oxide or silicon oxide; and the planarized metal portions are comprised of copper, aluminum or gold.

4. (Currently Amended) The method of claim 2 [[1]], wherein the metal structure is comprised of copper; the dielectric layer is comprised of an oxide material having a dielectric constant of less than about 3.0; the top layer is comprised of silicon oxynitride; the bottom electrodes are comprised of TaN or TiN; the capacitance dielectric layer is comprised of oxide; and the planarized metal portions are comprised of copper.

5. (Currently Amended) The method of claim 2 [[1]], wherein the metal structure has a thickness of from about 1000 to 9000Å; the dielectric layer has a thickness of from about 2000 to 12,000Å; the top layer has a thickness of from about 300 to 1500Å; the bottom electrodes have a thickness of from about 100 to 500Å; and the capacitance dielectric layer has a thickness of from about 100 to 600Å.

6. (Currently Amended) The method of claim 2 [[1]], wherein the metal structure has a thickness of from about 2000 to 8000Å; the dielectric layer has a thickness of from about 7000 to 9000Å; the top layer has a thickness of from about 1000 to 14,000Å; the bottom electrodes have a thickness of from about 200 to 400Å; and the capacitance dielectric layer has a thickness of from about 250 to 350Å.

7. (Currently Amended) The method of claim 2 [[1]], further including the step of forming a etch stop layer between the metal structure and the dielectric layer.

8. (Currently Amended) The method of claim 1, further including the step of forming a etch stop layer between the metal structure and the dielectric layer; the etch stop layer being comprised or silicon nitride or silicon carbide and having a thickness of from about 300 to 900Å.

9. (Currently Amended) The method of claim 1, further including the step of forming a etch stop layer between the metal structure and the dielectric layer; the etch stop layer being comprised of silicon nitride or silicon carbide and having a thickness of from about 400 to 600Å.

10. (Currently Amended) The method of claim 2 [[1]], wherein the initial via openings expose portions of the metal structure.

11. (Original) The method of claim 1, further including a top metal process.

12. (Original) A method of forming a MIM capacitor, comprising the sequential steps of:

providing a structure having a metal structure formed thereover; the metal structure being comprised of copper, aluminum or gold;

forming a dielectric layer over the metal structure; the dielectric layer being comprised of an oxide material having a dielectric constant of less than about 3.0, silicon oxide or FSG;

forming a top layer over the dielectric layer; the top layer being comprised of silicon oxynitride;

forming a capacitance trench through the top layer and into the dielectric layer; the capacitance trench have opposing side walls and a bottom;

forming respective bottom electrodes over the capacitance trench opposing side walls; the bottom electrodes being comprised of TaN or TiN;

forming a capacitance dielectric layer over the respective bottom electrodes, the bottom of the capacitance trench; and the remaining top layer; the capacitance dielectric layer being comprised of oxide or silicon oxide;

forming respective opposing initial via openings adjacent the capacitance trench;

forming respective trench openings above, continuous and contiguous with the lower portions of the respective opposing initial via openings and exposing portions of the underlying metal structure to form respective opposing dual damascene openings; and

forming planarized metal portions within:

the dual damascene openings; and

the capacitance trench to form a top electrode;

the planarized metal portions being comprised of copper, aluminum or gold; to complete formation of the MIM capacitor.

13. (Original) The method of claim 12, wherein the structure is a silicon substrate, a germanium substrate, a semiconductor wafer or a semiconductor substrate.

14. (Original) The method of claim 12, wherein the metal structure is comprised of copper; the dielectric layer is comprised of an oxide material having a dielectric constant of less than about 3.0; the top layer is comprised of silicon oxynitride; the bottom electrodes are comprised of TaN or TiN; the capacitance dielectric layer is comprised of oxide; and the planarized metal portions are comprised of copper.

15. (Original) The method of claim 12, wherein the metal structure has a thickness of from about 1000 to 9000Å; the dielectric layer has a thickness of from about 2000 to 12,000Å; the top layer has a thickness of from about 300 to 1500Å; the bottom electrodes have a thickness of about 100 to 500Å; and the capacitance dielectric layer has a thickness of from about 100 to 600Å.

16. (Original) The method of claim 12, wherein the metal structure has a thickness of from about 2000 to 8000Å; the dielectric layer has a thickness of from about 7000 to 9000Å; the top layer has a thickness of from about 1000 to 14,000Å; the bottom electrodes have a thickness

of from about 200 to 400Å; and the capacitance dielectric layer has a thickness of from about 250 to 350Å.

17. (Original) The method of claim 12, including the step of forming a etch stop layer between the metal structure and the dielectric layer.

18. (Original) The method of claim 12, including the step of forming a etch stop layer between the metal structure and the dielectric layer; the etch stop layer being comprised of silicon nitride or silicon carbide and having a thickness of from about 300 to 900Å.

19 (Original) The method of claim 12, including the step of forming a etch stop layer between the metal structure and the dielectric layer; the etch stop layer being comprised of silicon nitride or silicon carbide and having a thickness of from about 400 to 600Å.

20 (Original) The method of claim 12, wherein the initial via openings expose portions of the metal structure.

21. (Original) The method of claim 12, further including a top metal process.

22. (Original) A vertical MIM capacitor, comprising:

a bottom structure having a metal structure formed thereover;

a patterned dielectric layer over the metal structure;

a metal-insulator-metal structure within the patterned dielectric layer; the metal-insulator-metal structure having a first and second opposing sides;

a first planarized metal portion adjacent the metal-insulator-metal structure on the first opposing side; the first planarized metal portion being in electrical connection with the metal structure;

a second planarized metal portion adjacent the metal-insulator-metal structure on the second opposing side;

an inter-metal dielectric layer over the metal-insulator-metal structure and the first and second planarized metal portion; and

a contact within the inter-metal dielectric layer in electrical contact with the second planarized metal portion.

23 (Original) The structure of claim 22, wherein the bottom structure is a silicon substrate, a germanium substrate, a semiconductor wafer or a semiconductor substrate.

24. (Original) The structure of claim 22, wherein the metal structure is comprised of copper, aluminum or gold; the patterned dielectric layer is comprised of an oxide material having a dielectric constant of less than about 3.0, silicon oxide or FSG; and the planarized metal portions are comprised of copper, aluminum or gold.

25. (Original) The structure of claim 22, wherein the metal structure is comprised of copper; the dielectric layer is comprised of an oxide material having a dielectric constant of less than about 3.0; and the planarized metal portions are comprised of copper.

26. (Original) The structure of claim 22, wherein the metal structure has a thickness of from about 1000 to 9000Å; and the patterned dielectric layer has a thickness of from about 2000 to 12,000Å.

27. (Original) The structure of claim 22, wherein the metal structure has a thickness of from about 2000 to 8000Å; and the dielectric layer has a thickness of from about 7000 to 9000Å.

28. (Original) The structure of claim 22, including a pair of respective bottom electrodes interposed between the metal-insulator-metal structure and the first and second planarized metal portions.

29. (Original) The structure of claim 22, including a pair of respective bottom electrodes interposed between the metal-insulator metal structure and the first and second planarized metal portions; the pair of respective bottom electrodes each being comprised of TaN or TiN and having a thickness of from about 100 to 500Å.

30. (Original) The structure of claim 22, including a pair of respective bottom electrodes interposed between the metal-insulator-metal structure and the first and second planarized metal portions; the pair of respective bottom electrodes each being comprised of TaN and TiN and having a thickness of from about 200 to 400Å.

31. (New) The method of claim 1, wherein the structure is a silicon substrate, a germanium substrate, a semiconductor wafer or a semiconductor substrate.